UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,018	08/22/2003	Zahi Said Abuhamdeh	TRA-078	1441

36822 7590 09/11/2007

GORDON & JACOBSON, P.C.
60 LONG RIDGE ROAD
SUITE 407
STAMFORD, CT 06902

EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2117	
MAIL DATE	DELIVERY MODE
09/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/647,018
Filing Date: August 22, 2003
Appellant(s): ABUHAMDEH ET AL.

David P. Gordon
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 05/31/2007 appealing from the Office action mailed 08/10/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Texas Instruments, "IEEE Std. 1149.1 (JTAG) TAP Masters with 8-bit generic host interfaces, embedded test-bus controllers"; SCBS676D - December 1996 - Revised August 2002.

Patavalis, "A Brief Introduction to the JTAG Boundary Scan Interface", inAccess networks, Athens, November 8, 2001, pages 1-6.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

a) The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

b) The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

c) Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Texas Instruments (IEEE Std. 1149.1 (JTAG) TAP Masters with 8-bit generic host interfaces, embedded test-bus controllers; SCBS676D – December 1996-Revised August 2002) in view of Patavalis (A Brief Introduction to the JTAG Boundary Scan Interface, pages 1-6, Athens, November 8, 2001).

As per claim 1, Texas Instruments teaches an integrated circuit chip, comprising: c) an on-chip JTAG master coupled to said JTAG TAP; and d) an on-chip microprocessor interface coupled to said JTAG master (fig. 1, 3, 4, 5, pages 1-9, Texas Instruments). The examiner would like to point out that the Embedded Test Bust Controller (eTBC) in Texas Instruments is similar to JTAG master.

However Texas Instruments does not explicitly teach the specific use of a) core logic; b) an on-chip JTAG TAP coupled to said core logic.

Patavalis in an analogous art teaches JTAG Boundary Scan Interface Architecture in fig. 1 that includes core logic connected to JTAG TAP (page 2, Patavalis). Patavalis teaches that all the signals between the chip's core logic and the pins are intercepted by a serial scan path (page 2, Patavalis).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Texas Instruments' document with the teachings of Patavalis by including an additional step of using a) core logic; b) an on-chip JTAG TAP coupled to said core logic.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a) core logic; b) an on-chip JTAG TAP coupled to said core logic would provide the opportunity to access and control the signal-levels on the pins of a digital circuit and test the internal circuitry on the chip.

- As per claim 2, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, further comprising: e) a plurality of registers coupled to said microprocessor interface and to said JTAG master (pages 12, 16, Texas Instruments).

- As per claim 3, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said plurality of registers includes a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register (pages 12, 16, 24, 25, Texas Instruments).

- As per claim 4, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said plurality of registers includes a start bit register and an end bit register (pages 14, 15, Texas Instruments).

- As per claim 5, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said chip has more than five pins and five of said pins are coupled to said on-chip JTAG TAP forming a JTAG interface to said chip (fig. 1, pages 1-5, Texas Instruments).

- As per claim 6, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, further comprising: e) switching means for selectively decoupling said JTAG interface from said JTAG TAP (page 13, Texas Instruments).

- As per claim 7, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said switching means is coupled to and controllable by said JTAG master (fig. 1, pages 5, 9, 13, Texas Instruments).

- As per claim 8, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said switching means couples said JTAG master to said JTAG TAP when said JTAG interface is decoupled from said JTAG TAP, and said switching means couples said JTAG interface to said JTAG TAP when said JTAG master is decoupled from said JTAG TAP (fig. 1, pages 5, 6, 9, 13, Texas Instruments).

- As per claim 9, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches an integrated circuit chip, comprising: c) an on-chip JTAG interface selectively coupled to said JTAG TAP; d) an on-chip microprocessor interface selectively coupled to said JTAG TAP; and e) switching means for selectively coupling said JTAG interface and said microprocessor interface to said JTAG TAP (fig. 1, pages 5, 6, 9, 13, Texas Instruments).

Patavalis teaches a) core logic; b) an on-chip JTAG TAP coupled to said core logic ("JTAG Boundary Scan Interface Architecture" in fig. 1, page 2, Patavalis).

- As per claim 10, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said switching means operates to decouple said JTAG interface from said JTAG TAP when said microprocessor interface is coupled to said JTAG TAP, and said switching means operates to decouple said microprocessor interface from said JTAG TAP when said JTAG interface is coupled to said JTAG TAP (fig. 1, pages 5, 6, 9, 13, Texas Instruments).

- As per claim 11, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said microprocessor interface includes a plurality of registers (pages 12, 16, Texas Instruments).

- As per claim 12, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said switching means is controllable via said microprocessor interface (fig. 1, pages 5, 9, 13, Texas Instruments).

- As per claim 13, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, further comprising: f) a switching means enable interface for receiving a signal to enable said switching means, wherein said switching means is inoperable without receiving said signal (discrete control and multiplexers in the functional block diagram on page 3, page 16, Texas Instruments).

- As per claim 14, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: in the absence of said signal said switching means decouples said microprocessor interface from said JTAG TAP and couples said JTAG interface to said JTAG TAP (fig. 1, the functional block diagram on page 3, pages 5, 6, Texas Instruments).
16, Texas Instruments).

- As per claim 15, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said plurality of registers includes a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register (pages 12, 16, 24, 25, Texas Instruments).

- As per claim 16, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said TDI FIFO and said TMS FIFO each being N-bits in size, and said microprocessor interface includes means for performing TAP operations having bit counts in excess of N-bits (fig. 1, pages 5, 16, 24, 25, Texas Instruments).

- As per claim 17, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: means for performing TAP operations having bit counts in excess of N-bits includes means for cycling said TAP through state elements and holding it in one of four states (fig. 8, tables 7-12, pages 19-24, Texas Instruments).

- As per claim 18, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said four states include Test-logic Reset, Run-Test Idle, Pause-IR, and Pause-DR (table 12, pages 21, 23, 24, Texas Instruments).

- As per claim 19, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches an integrated circuit chip comprising: c) an on-chip JTAG master selectively coupled to said JTAG TAP; d) an on-chip JTAG interface selectively coupled to said JTAG TAP; and e) switching means for selectively coupling said JTAG master and said JTAG interface to said JTAG TAP (fig. 1, pages 5, 6, 9, 13, Texas Instruments).
Patavalis teaches a) core logic; b) an on-chip JTAG TAP coupled to said core logic ("JTAG Boundary Scan Interface Architecture" in fig. 1, page 2, Patavalis).

- As per claim 20, Texas Instruments and Patavalis teach the additional limitations.

Texas Instruments teaches the chip, wherein: said switching means operates to decouple said JTAG interface from said JTAG TAP when said JTAG master is coupled to said JTAG. TAP, and said switching means operates to decouple said JTAG master from said JTAG TAP when said JTAG interface is coupled to said JTAG TAP (fig. 1, pages 5, 6, 9, 13, Texas Instruments).

(10) Response to Argument

i) Claim 1

Appellant argues that claim 1 calls for a JTAG TAP and JTAG master to be on the same chip with the core logic. The prior art does not teach or suggest combining these elements on a single chip.

The examiner disagrees. Texas Instruments teaches that eTBC's function is to master an IEEE Std 1149.1 (JTAG) test access port (TAP) under the command of an embedded host microprocessor/microcontroller (page 1, description, Texas Instruments). The examiner would like to point out that the Embedded Test Bus Controller (eTBC) in Texas Instruments' document is similar to a JTAG master. Texas Instruments teaches that the eTBC masters all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset (TRST). All such signals can be connected directly to the associated target IEEE Std 1149.1 devices without need for additional logic or buffering (page 2, paragraph 1, Texas Instruments). Texas Instruments also teaches that the eTBC operates as a simple 8-bit memory- or I/O-mapped peripheral to a microprocessor/microcontroller (host). High-level commands and parallel data are passed to/from the eTBC via the generic host interface, which includes and 8-bit data bus (D7-D0) and a 3-bit address bus (A2-A0), page 2, paragraph 2, Texas Instruments. Texas Instruments teaches that a discrete mode is also available in which the TAP is driven strictly by read/write cycles under full control of the microprocessor/microcontroller host (page 2, paragraph 6, Texas Instruments).

Patavalis teaches JTAG Boundary Scan Interface Architecture in figure 1 that includes core logic connected to a JTAG TAP on an integrated circuit chip (figure 1, page 2, Patavalis).

It would have obvious to one having ordinary skill in the art to combine a JTAG TAP and JTAG master to be on the same chip with the core logic as a JTAG master (eTBC) can master all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test

data input (TDI), test data output (TDO), and test reset (TRST) directly under full control of the microprocessor/microcontroller host without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

ii) Claim 2

Appellant argues that claim 2 specifies that the chip also contains a plurality of registers coupled to the microprocessor interface and to the JTAG master. The fact that the elements in the prior art are on separate chips is ignored by the Examiner. Therefore, claim 2 is patentable over the art of record.

The examiner respectfully disagrees. Appellant is arguing the references separately and not their combined teachings. As discussed above, Patavalis teaches JTAG Boundary Scan Interface Architecture in figure 1 that includes core logic connected to a JTAG TAP and JTAG interface on an **integrated (i.e. single) circuit chip** (figure 1, JTAG Boundary Scan Interface Architecture page 2, Patavalis). Patavalis teach JTAG interface signals TRST, TCK, TMS, TDI and TDO (page 3, Patavalis).

Texas Instruments teaches that a summary of the eTBC registers, their address mappings, bit assignments, reset values, and host accessibility (read/write or read-only) is provided in Table 1. All registers are fully readable by the host (table 1, page 12, paragraph 1, Texas Instruments).

iii) Claim 3

Appellant argues that claim 3 specifies what kind of registers (a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register) are included on the chip and these are some of the registers used in performing the JTAG boundary scan. While these registers are known in the art, the art neither teaches nor suggests that they be on the same chip as the TAP and the master and the core logic. Therefore claim 3 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches that a summary of the eTBC registers, TDO buffer register, TDI buffer register and Counter register is provided in Table 1. All registers are fully readable by the host (page 12, paragraph 1, Texas Instruments). Texas Instruments teach that the counter register, while only 8 bits wide like any other eTBC register, provides read/write access to the full 32-bit eTBC counter (page 16, paragraph 1, Texas Instruments). Texas Instruments

teach that the TDO-buffer register, while only 8 bits wide like any other eTBC register, provides write access to the full 4x8 (32-bit) FIFO that comprises the TDO buffer (page 16, paragraph 2, Texas Instruments). Texas Instruments teach that the TDI-buffer register, while only 8 bits wide like any other eTBC register, provides read access to the full 4x8 (32-bit) FIFO that comprises the TDI buffer (page 16, paragraph 3, Texas Instruments). Texas Instruments teach that the eTBC generates a TMS sequence to move the target scan chain from its current TAP state to a working state that depends on the test objective (page 17, paragraph 3, Texas Instruments). The examiner would like to point out that these registers are on a single chip that includes eTBC that masters all TAP signals required to support one 4- or 5-wire IEEE Std 1149.1 serial test bus directly under full control of the microprocessor/microcontroller host (page 3, eTBC functional block diagram, page 2, paragraph 1, Texas Instruments).

iv) Claim 4

Appellant argues that claim 4 specifies that the registers include a start bit register and an end bit register. The Examiner refers to pages 14 and 15 of Texas Instruments, which describe various registers. However, none of the registers is a start bit register or an end bit register. The combination of art cited by the Examiner therefore fails to even recite all of the claimed limitations. Therefore claim 4 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches that Texas Instruments teaches that the test-reset (TRST) bit allows direct software control of the state of the TRST output in modes other than discrete control (page 15, table 5, paragraph 1, Texas Instruments). Texas Instruments also teaches that the end-TAP-state (ENDST) bit group determines the TAP state in which the target scan chain is left when the requested command finishes (page 15, table 5, paragraph 2, Texas Instruments). The examiner would like to point out TRST (start bit) and ENDST (end bit) are in command register for eTBC.

v) Claim 5

Appellant argues that claim 5 specifies that the chip has more than five pins and five of the pins (TRST, TMS, TCK, TDI, and TDO) are coupled to the on-chip JTAG TAP 14 forming a JTAG interface to said chip

10. In rejecting claim 5, the Examiner refers to Figure 1 of Texas Instruments, implying that the components shown are all on a single chip. This is clearly not the case, however. All known prior implementations of the JTAG standard provide the TAP and the master on separate chips. Moreover, the JTAG interface is essentially a TAP for use by an off-chip master. Thus, the chip has two TAPS, one internal to be used by an on-chip master and one defined by the five pins for use with an off-chip master. No chip in the prior art shows two TAPs on the same chip. The combination of art cited by the Examiner fails to even recite all of the claim limitations. Therefore claim 5 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner' s rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches that the chip has more than five pins and five of the pins are TRST, TMS, TCK, TDI, and TDO (fig. 1, page 5, Texas Instruments).

Patavalis teaches chip has more than five pins and five of said pins are coupled to said on-chip JTAG TAP forming a JTAG interface to said chip (fig. 1, page 2, JTAG Boundary Scan Interface Architecture).

vi) Claim 6

Appellant argues that claim 6 adds the switching means 22, 24, 26, 36 in Figure 2 to claim 5 so that the JTAG interface (TRST, TMS, TCK, TDI, and TDO) can be decoupled from the JTAG TAP 14. In rejecting claim 6, the Examiner refers to page 13 of Texas Instruments, which specifies that the host can disable the output of the target, the host being the microprocessor in Figure 1, page 5 and the target being the device under test. The prior art does not teach or suggest placing the switching means on the same chip as the TAP and the master. According to the prior art, an external register and external microprocessor are required to switch off the output of the TAP. Therefore claim 6 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches that the negated test-output-enable (NTOE) bit allows the host to disable the TAP outputs via software in a manner analogous to the hardware TOE (page 13, paragraph 1, Texas Instruments). Texas Instruments also teaches that

the eTBC's test-output enable allows its master function to be disabled so that another device (an external tester, for example) can control the target TAP (page 6, paragraph 1, Texas Instruments).

Texas Instruments teach the JTAG master (eTBC) (fig. 1, page 1, 5, Texas Instruments) and the switching means on a chip (page 6, paragraph 1, page 13, paragraph 1, Texas Instruments). Patavalis teach JTAG TAP and JTAG interface on a chip (fig. 1, JTAG Boundary Scan Interface Architecture, page 2, Patavalis).

It would have obvious to one having ordinary skill in the art to place the switching means on the same chip as the TAP and the master as the eTBC (master) can master all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

vii) Claim 7

Appellant argues that Claim 7 further specifies that the switching means is coupled to and controllable by the JTAG master 16, which, as specified in parent claim 1, is on the same chip. According to the cited portion of Texas Instruments, the switching means is not controlled by the JTAG master but is controlled by the host (microprocessor) and the host, the master, and the TAP are all on separate chips. Therefore claim 7 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches to disable the eTBC (master) so that an external controller can master the associated IEEE Std 1149.1 test bus (page 2, paragraph 7, Texas Instruments).

Texas Instruments teach the JTAG master (eTBC) (fig. 1, page 1, 5, Texas Instruments) and the switching means on a chip (page 6, paragraph 1, page 13, paragraph 1, Texas Instruments). Patavalis teach JTAG TAP and JTAG interface on a chip (fig. 1, JTAG Boundary Scan Interface Architecture, page 2, Patavalis).

It would have obvious to one having ordinary skill in the art to place the switching means on the same chip as the TAP and the master as the eTBC (master) can master all TAP signals required to support one

4-or 5-wire IEEE Std 1149.1 serial test bus without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

viii) Claim 8

Appellant argues that Claim 8 specifies that the switching means couples the JTAG master 16 to the JTAG TAP 14 when the JTAG interface (TRST, TMS, TCK, TDI, and TDO) is decoupled from the JTAG TAP, and couples the JTAG interface to the JTAG TAP when the JTAG master is decoupled from the JTAG TAP. The Examiner refers to Texas Instruments Fig. 1, and pages 5, 6, 9, and 13. However, the only teaching in Texas Instruments regarding switching is the toggling of the NTOE bit, which toggles the TAP output on and off. This substantially decouples the TAP from the master, but it does not couple the TAP to anything else. Moreover, the switching means described by Texas Instruments is not on a single chip together with the TAP, the master, and the JTAG interface. In addition, Texas Instruments does not disclose or suggest a JTAG interface other than the TAP. As the term is defined in the specification and as can be gleaned from Figure 1 of the application, the JTAG interface is an extension of the on-chip TAP to five pins on the chip. This allows the chip to be used in a conventional manner, i.e. with an off-chip JTAG master, when the switching means couples the JTAG interface to the JTAG TAP. It also allows the chip to be used in the inventive way when the switching means couples the JTAG master 16 to the JTAG TAP 14. Therefore claim 8 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection. The examiner disagrees and would like to point out that Texas Instruments teaches that the negated test-output-enable (NTOE) bit allows the host to disable the TAP outputs via software in a manner analogous to the hardware TOE (page 13, paragraph 1, Texas Instruments). Texas Instruments also teaches that the eTBC's test-output enable allows its master function to be disabled so that another device (an external tester, for example) can control the target TAP (page 6, paragraph 1, Texas Instruments). Texas Instruments teach the JTAG master (eTBC) (fig. 1, page 1, 5, Texas Instruments) and the switching means on a chip (page 6, paragraph 1, page 13, paragraph 1, Texas Instruments). Patavalis teach JTAG TAP and JTAG interface on a chip (fig. 1, JTAG Boundary Scan Interface Architecture, page 2, Patavalis).

It would have obvious to one having ordinary skill in the art to place the switching means on the same chip as the TAP, the master and the JTAG interface as the eTBC (master) can master all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

ix) Claims 9 and 12

Appellant argues that independent claim 9 is drawn to an integrated circuit chip having core logic, an on-chip JTAG TAP, an on-chip JTAG interface, an on-chip microprocessor interface, and switching means for selectively coupling the TAP to either the JTAG interface or the microprocessor interface. As described above with respect to claim 8, the only switching means shown in the prior art is the NTOE bit toggling which requires three chips and which does not couple the TAP to anything else when it is decoupled from the master. In addition, the prior art does not show a TAP, a JTAG interface, and a microprocessor interface all on the same chip. The Examiner's alleged incentive for combining JTAG elements on the same chip is not a true incentive as the goals stated in the incentive are already accomplished by the prior art without the combination on the same chip. In addition Texas Instruments and Patavalis teach away from combining these elements on the same chip. Therefore claim 9 and claim 12, which depends therefrom, are patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches that the negated test-output-enable (NTOE) bit allows the host to disable the TAP outputs via software in a manner analogous to the hardware TOE (page 13, paragraph 1, Texas Instruments). Texas Instruments also teaches that the eTBC's test-output enable allows its master function to be disabled so that another device (an external tester, for example) can control the target TAP (page 6, paragraph 1, Texas Instruments). Texas Instruments teaches that the eTBC's function is to master an IEEE Std 1149.1 (JTAG) test access port (TAP) under the command of an embedded host microprocessor/microcontroller (page 1, Texas Instruments).

Patavalis teaches JTAG Boundary Scan Interface Architecture in figure 1 that includes core logic connected to a JTAG TAP and JTAG interface on an integrated circuit chip (figure 1, JTAG Boundary Scan Interface Architecture page 2, Patavalis). Patavalis teach JTAG interface signals TRST, TCK, TMS, TDI and TDO (page 3, Patavalis).

It would have obvious to one having ordinary skill in the art to combine a JTAG TAP and JTAG interface to be on the same chip with the microprocessor interface as a JTAG master (eTBC) can master all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset (TRST) directly under full control of the microprocessor/microcontroller host without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

x) Claim 10

Appellant argues that claim 10 further clarifies that the switching means decouples the TAP from the JTAG interface when the TAP is coupled to the microprocessor interface and decouples the TAP from the microprocessor interface when the TAP is coupled to the JTAG interface. As described above, the only switching means shown in the prior art is the NTOE bit toggling which requires three chips and which does not couple the TAP to anything else when it is decoupled from the master. Therefore claim 10 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches that the negated test-output-enable (NTOE) bit allows the host to disable the TAP outputs via software in a manner analogous to the hardware TOE (page 13, paragraph 1, Texas Instruments). Texas Instruments also teaches that the eTBC's test-output enable allows its master function to be disabled so that another device (an external tester, for example) can control the target TAP (page 6, paragraph 1, Texas Instruments). Texas Instruments teaches that the eTBC's function is to master an IEEE Std 1149.1 (JTAG) test access port (TAP) under the command of an embedded host microprocessor/microcontroller (page 1, Texas Instruments).

Patavalis teaches JTAG Boundary Scan Interface Architecture in figure 1 that includes core logic connected to a JTAG TAP and JTAG interface on an integrated circuit chip (figure 1, JTAG Boundary Scan Interface Architecture page 2, Patavalis). Patavalis teach JTAG interface signals TRST, TCK, TMS, TDI and TDO (page 3, Patavalis).

It would have obvious to one having ordinary skill in the art to combine a JTAG TAP and JTAG interface to be on the same chip with the microprocessor interface as a JTAG master (eTBC) can master all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset (TRST) directly under full control of the microprocessor/microcontroller host without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

xi) Claim 11

Appellant argues that claim 11 further specifies that the microprocessor interface includes a plurality of registers. As shown in the prior art, these registers are provided on yet another chip separate from the chip containing the TAP and the chip containing the microprocessor. There is no suggestion in the prior art to put all of these components on a single chip. Therefore claim 11 is allowable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner' s rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches that a summary of the eTBC registers, their address mappings, bit assignments, reset values, and host accessibility (read/write or read-only) is provided in Table 1. All registers are fully readable by the host (table 1, page 12, paragraph 1, Texas Instruments).

Patavalis teaches JTAG Boundary Scan Interface Architecture in figure 1 that includes core logic connected to a JTAG TAP and JTAG interface on an integrated circuit chip (figure 1, JTAG Boundary Scan Interface Architecture page 2, Patavalis). Patavalis teach JTAG interface signals TRST, TCK, TMS, TDI and TDO (page 3, Patavalis).

It would have obvious to one having ordinary skill in the art to combine a JTAG TAP and JTAG interface to be on the same chip with eTBC and the microprocessor interface including a plurality of registers as a

JTAG master (eTBC) can master all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset (TRST) directly under full control of the microprocessor/microcontroller host without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

xii) Claims 13 and 14

Appellant argues that claim 13 further specifies a switching means enable interface, which enables or disables the switching means. As described above, the only switching means shown in the prior art is the NTOE bit toggling which requires three chips and which does not couple the TAP to anything else when it is decoupled from the master. Moreover, there is no switching means enable interface shown in the prior art. Therefore claim 13 and claim 14, which is dependent therefrom, are patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches that the negated test-output-enable (NTOE) bit allows the host to disable the TAP outputs via software in a manner analogous to the hardware TOE (page 13, paragraph 1, Texas Instruments). Texas Instruments also teaches that the eTBC's test-output enable allows its master function to be disabled so that another device (an external tester, for example) can control the target TAP (page 6, paragraph 1, Texas Instruments). Texas Instruments teaches that the eTBC's function is to master an IEEE Std 1149.1 (JTAG) test access port (TAP) under the command of an embedded host microprocessor/microcontroller (page 1, Texas Instruments).

Patavalis teaches JTAG Boundary Scan Interface Architecture in figure 1 that includes core logic connected to a JTAG TAP and JTAG interface on an integrated circuit chip (figure 1, JTAG Boundary Scan Interface Architecture page 2, Patavalis). Patavalis teach JTAG interface signals TRST, TCK, TMS, TDI and TDO (page 3, Patavalis).

It would have obvious to one having ordinary skill in the art to combine a JTAG TAP and JTAG interface to be on the same chip with the microprocessor interface as a JTAG master (eTBC) can master all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode

select (TMS), test data input (TDI), test data output (TDO), and test reset (TRST) directly under full control of the microprocessor/microcontroller host without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

xiii) Claim 15

Appellant argues that claim 15 specifies that the on-chip registers include a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register. As described above, state of the art JTAG implementations put these registers in a separate chip. See Figure 1 of Texas Instruments. Therefore claim 15 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner' s rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches that a summary of the eTBC registers, TDO buffer register, TDI buffer register and Counter register is provided in Table 1. All registers are fully readable by the host (page 12, paragraph 1, Texas Instruments). Texas Instruments teach that the counter register, while only 8 bits wide like any other eTBC register, provides read/write access to the full 32-bit eTBC counter (page 16, paragraph 1, Texas Instruments). Texas Instruments teach that the TDO-buffer register, while only 8 bits wide like any other eTBC register, provides write access to the full 4x8 (32-bit) FIFO that comprises the TDO buffer (page 16, paragraph 2, Texas Instruments). Texas Instruments teach that the TDI-buffer register, while only 8 bits wide like any other eTBC register, provides read access to the full 4x8 (32-bit) FIFO that comprises the TDI buffer (page 16, paragraph 3, Texas Instruments). Texas Instruments teach that the eTBC generates a TMS sequence to move the target scan chain from its current TAP state to a working state that depends on the test objective (page 17, paragraph 3, Texas Instruments).

Patavalis teaches JTAG Boundary Scan Interface Architecture in figure 1 that includes core logic connected to a JTAG TAP and JTAG interface on an integrated circuit chip (figure 1, JTAG Boundary Scan Interface Architecture page 2, Patavalis). Patavalis teach JTAG interface signals TRST, TCK, TMS, TDI and TDO (page 3, Patavalis).

It would have obvious to one having ordinary skill in the art to combine a JTAG TAP and JTAG interface to be on the same chip with eTBC and the microprocessor interface including a plurality of registers as a

JTAG master (eTBC) can master all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset (TRST) directly under full control of the microprocessor/microcontroller host without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

xiv) Claim 16

Appellant argues that claim 16 specifies that the size of the registers are each N-bits and that the microprocessor interface includes means for performing TAP operations having bit- counts in excess of N-bits. The Examiner refers to several pages in Texas Instruments, which discuss registers, but it appears that the TAP operations described are limited to the size of the registers, i.e. 32-bits. Therefore claim 16 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

The examiner disagrees and would like to point out that Texas Instruments teaches that a summary of the eTBC registers, TDO buffer register, TDI buffer register and Counter register is provided in Table 1. All registers are fully readable by the host (page 12, paragraph 1, table 1, Texas Instruments). Texas Instruments teach that the TDO-buffer register, while only 8 bits wide like any other eTBC register, provides write access to the full 4x8 (32-bit) FIFO that comprises the TDO buffer. The TDO-buffer register can be written as long as the TDO buffer does not become full (page 16, paragraph 2, Texas Instruments). Texas Instruments teach that the TDI-buffer register, while only 8 bits wide like any other eTBC register, provides read access to the full 4x8 (32-bit) FIFO that comprises the TDI buffer. The TDI-buffer register can be read as long as the TDI buffer does not become empty (page 16, paragraph 3, Texas Instruments). The examiner would like to point out that as the TDO-buffer register can be written as long as the TDO buffer does not become full and TDI-buffer register can be read as long as the TDI buffer does not become empty, the microprocessor interface means performs TAP operations having bit counts in excess of N-bits.

xv) Claims 17 and 18

Appellant argues that claim 17 specifies that the means for performing TAP operations having bit- counts in excess of N-bits includes means for cycling the TAP through states. While Texas Instruments

discusses TAP states required by the JTAG standard, there is no discussion of how to use these states to perform operations having bit counts in excess of the register size. Therefore claim 17 and claim 18, which depends therefrom, are patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness.

The examiner disagrees and would like to point out that Texas Instruments teaches means for cycling TAP through state elements and holding it in one of four states (page 19, 22, fig. 8, Texas Instruments). Texas Instruments teaches that the TDO-buffer register, while only 8 bits wide like any other eTBC register, provides write access to the full 4x8 (32-bit) FIFO that comprises the TDO buffer. The TDO-buffer register can be written as long as the TDO buffer does not become full (page 16, paragraph 2, Texas Instruments). Texas Instruments teach that the TDI-buffer register, while only 8 bits wide like any other eTBC register, provides read access to the full 4x8 (32-bit) FIFO that comprises the TDI buffer. The TDI-buffer register can be read as long as the TDI buffer does not become empty (page 16, paragraph 3, Texas Instruments). The examiner would like to point out that as the TDO-buffer register can be written as long as the TDO buffer does not become full and TDI-buffer register can be read as long as the TDI buffer does not become empty, the microprocessor interface means performs TAP operations having bit counts in excess of N-bits.

xvi) Claims 19 and 20

Appellant argues that independent claim 19 is drawn to an integrated circuit chip having core logic, an on-chip JTAG TAP, an on-chip JTAG master, an on-chip JTAG interface, and switching means for selectively coupling the JTAG master and the JTAG interface to the JTAG TAP. The Examiner's rejection of claim 19 is essentially the same as his rejection of claim 1 and the remarks made above regarding claim 1 apply to claim 19 as well. In addition, the only switching means shown in the prior art is the NTOE bit toggling which requires three chips and which does not couple the TAP to anything else when it is decoupled from the master. Therefore claim 19 and claim 20, which depends therefrom, are patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

The examiner disagrees. Texas Instruments teaches that eTBC's function is to master an IEEE Std 1149.1 (JTAG) test access port (TAP) under the command of an embedded host microprocessor/microcontroller (page 1, description, Texas Instruments). The examiner would like to point out that the Embedded Test Bus Controller (eTBC) in Texas Instruments' document is similar to a JTAG master. Texas Instruments teaches that the eTBC masters all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset (TRST). All such signals can be connected directly to the associated target IEEE Std 1149.1 devices without need for additional logic or buffering (page 2, paragraph 1, Texas Instruments). Texas Instruments also teaches that the eTBC operates as a simple 8-bit memory- or I/O-mapped peripheral to a microprocessor/microcontroller (host). High-level commands and parallel data are passed to/from the eTBC via the generic host interface, which includes and 8-bit data bus (D7-D0) and a 3-bit address bus (A2-A0), page 2, paragraph 2, Texas Instruments. Texas Instruments teaches that a discrete mode is also available in which the TAP is driven strictly by read/write cycles under full control of the microprocessor/microcontroller host (page 2, paragraph 6, Texas Instruments).

Texas Instruments teaches that the negated test-output-enable (NTOE) bit allows the host to disable the TAP outputs via software in a manner analogous to the hardware TOE (page 13, paragraph 1, Texas Instruments). Texas Instruments also teaches that the eTBC's test-output enable allows its master function to be disabled so that another device (an external tester, for example) can control the target TAP (page 6, paragraph 1, Texas Instruments).

Patavalis teaches JTAG Boundary Scan Interface Architecture in figure 1 that includes core logic connected to a JTAG TAP on an integrated circuit chip (figure 1, page 2, Patavalis).

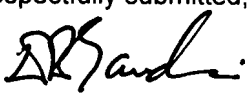
It would have obvious to one having ordinary skill in the art to combine a JTAG TAP and JTAG master to be on the same chip with the core logic as a JTAG master (eTBC) can master all TAP signals required to support one 4-or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset (TRST) directly under full control of the microprocessor/microcontroller host without need for additional logic or buffering and achieve the predictable results of reducing signal processing time.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



Dipakkumar Gandhi

Patent Examiner

8/29/2007

Conferees:

/Lynne H Browne/
Lynne H Browne
Appeal Practice Specialist, TQAS
Technology Center 2100

/Guy Lamarre/
Guy Lamarre

Primary Examiner

Art Unit 2112